Notice of Allowability	Application No.	Applicant(s)	
	09/882,760	LI ET AL.	
	Examiner	Art Unit	
	Andrew C. Lee	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *3/19/2007*.

2. ☒ The allowed claim(s) is/are *1-24*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Louis Sickles on 5/23/2007.

2. The application has been amended as follows:

- Claim 1 has been amended as following:

1. An MxN packet switch for switching M input packets arriving in each frame of a sequence of frame times to N output ports, the switch comprising:

an input module, having M inputs and B outputs, B > M, for switching the M input packets to M of the B outputs to produce M switched packets simultaneously during each ~~of the~~ frame of said sequence of frame times,

a packet buffer including B registers, coupled to the input module, for storing the M switched packets into M available registers during each ~~of the~~ frame of said sequence of frame times to produce M stored packets simultaneously, and

an output module, having B inputs and N outputs coupled to the packet buffer, for transferring up to N packets from occupied registers in each ~~of the~~ frame of said

sequence of frame times to the output ports simultaneously based upon destination addresses contained within each of the stored packets.

- Claim 10 has been amended as following:

10. An MxN packet switch for switching M input packets arriving in each frame of a sequence of frame times to N output ports, the switch comprising:

an MxB input crossbar switch, B > M, for switching the M input packets to M of the B outputs to produce M switched packets simultaneously during each ~~of the~~ frame of said sequence of frame times,

a one-stop shared buffer memory, including B registers, coupled to the input crossbar switch, for storing the M switched packets into M available registers during each ~~of the~~ frame of said sequence of frame times to produce M stored packets,

a BxN output crossbar switch coupled to the packet buffer, for transferring up to N packets from occupied registers in each ~~of the~~ frame of said sequence of frame times to the output ports simultaneously based upon destination addresses,

a register selector for assigning the M of the B registers during each ~~of the~~ frame of said sequence of frame times to generate M assigned registers,

M header hoppers, coupled to the input crossbar switch, for storing header information from each of the M input packets in each ~~of the~~ frame of said sequence of frame times and M addresses of the M assigned registers for the M input packets in each ~~of the~~ frame of said sequence of frame times, and

N queues for storing the addresses of the assigned registers in each ~~of the~~ frame

of said sequence of frame times as transmitted to the N queues from the M header hoppers based upon destination information in the header information.

- Claim 12 has been amended as following:

12. An MxN packet switch for switching M input packets arriving in each frame of a sequence of frame times to N output ports, the switch comprising:

input means, having M inputs and B outputs, B > M, for switching the M input packets to M of the B outputs to produce M switched packets simultaneously during each ~~of the~~ frame of said sequence of frame times,

storage means, including B registers, coupled to the input module, for storing the M switched packets into M available registers during each ~~of the~~ frame of said sequence of frame times to produce M stored packets simultaneously, and

output means, having B inputs and N outputs coupled to the packet buffer, for transferring up to N packets from occupied registers in each ~~of the~~ frame of said sequence of frame times to the output ports simultaneously based upon destination addresses contained within each of the stored packets.

- Claim 21 has been amended as following:

21. A method for switching M input packets arriving in each frame of a sequence of frame times to N output ports using an MxN packet switch, the method comprising:

switching the M input packets to M of the B outputs to produce M switched packets during each ~~of the~~ frame of said sequence of frame times, B > M,

storing the M switched packets into M of B registers during each ~~of the~~ frame of said sequence of frame times to produce M stored packets simultaneously, and

transferring up to N packets from up to N of the B registers in each ~~of the~~ frame of said sequence of frame times to the output ports simultaneously based upon destination information.

- Claim 23 has been amended as following:

23. A method for switching M input packets arriving in each frame of a sequence of frame times to N output ports using an MxN packet switch, the method comprising:

prior to the arrival of the M input packets in each ~~of the~~ frame of said sequence of frame times, selecting M available registers in a packet buffer having B registers, B > M, to store the M input packets simultaneously arriving in the next ~~one of the~~ frame of said sequence of frame times,

setting up connections in an input module to switch the M input packets to the M available registers,

transmitting the register addresses of the M available registers to header hoppers, delivering and storing the M input packets to the M available registers simultaneously using the connections of the input module,

sending headers from the M input packets to the header hoppers, transmitting the register addresses from the headers of the M input packets to N queues corresponding to destination addresses in the headers of the M input packets simultaneously,

updating the queues based on the header information provided by the header hoppers, sending control information to a register selector to inform the register selector of the destination addresses of the M input packets in each ~~of the~~ frame of said sequence of frame times,

selecting up to N stored packets from the packet buffer for each of the destination addresses based on contents of the queues,

transmitting the up to N selected stored packets to the outputs simultaneously, updating the register selector to account for any remaining destination addresses for each stored packet, and

transmitting any remaining stored packets to the N outputs in subsequent one or more subsequent frames to clear the remaining stored packets.

- Claim 24 has been amended as following:

24. (Original) A method for switching M input packets arriving in each frame of a sequence of frame times to N output ports using an MxN packet switch, the method comprising the steps of:

switching the M input packets to M of the B outputs to produce M switched packets simultaneously during each ~~of the~~ frame of said sequence of frame times, B > M,

storing the M switched packets into M of B registers during each ~~of the~~ frame of said sequence of frame times to produce M stored packets simultaneously, and

transferring up to N packets from up to N of the B registers in each ~~of the~~ frame

of said sequence of frame times to the output ports simultaneously based upon destination information.

REASONS FOR ALLOWANCE

3. Claims 1 – 24 are allowed over prior art.

4. The following is an examiner's statement of reasons for allowance:

The prior art of record, in single or in combination, does not disclose the limitations of

"a packet buffer including B registers, coupled to the input module, for storing the M switched packets into M available registers during each frame of said sequence of frame times to produce M stored packets simultaneously, and an output module, having B inputs and N outputs coupled to the packet buffer, for transferring up to N packets from occupied registers in each frame of said sequence of frame times to the output ports simultaneously based upon destination addresses contained within each of the stored packets" as disclosed in claim 1;

"a one-stop shared buffer memory, including B registers, coupled to the input crossbar switch, for storing the M switched packets into M available registers during each frame of said sequence of frame times to produce M stored packets, a BxN output crossbar switch coupled to the packet buffer, for transferring up to N packets from occupied registers in each frame of said sequence of frame times to the output ports simultaneously based upon destination addresses, a register selector for assigning the M of the B registers during each frame of said sequence of frame times to generate M

assigned registers, M header hoppers, coupled to the input crossbar switch, for storing header information from each of the M input packets in each frame of said sequence of frame times and M addresses of the M assigned registers for the M input packets in each frame of said sequence of frame times, and N queues for storing the addresses of the assigned registers in each frame of said sequence of frame times as transmitted to the N queues from the M header hoppers based upon destination information in the header information" as disclosed in claim 10;

"storage means, including B registers, coupled to the input module, for storing the M switched packets into M available registers during each frame of said sequence of frame times to produce M stored packets simultaneously, and output means, having B inputs and N outputs coupled to the packet buffer, for transferring up to N packets from occupied registers in each frame of said sequence of frame times to the output ports simultaneously based upon destination addresses contained within each of the stored packets" as disclosed in claim 12;

"storing the M switched packets into M of B registers during each frame of said sequence of frame times to produce M stored packets simultaneously, and transferring up to N packets from up to N of the B registers in each frame of said sequence of frame times to the output ports simultaneously based upon destination information" as disclosed in claim 21;

"prior to the arrival of the M input packets in each frame of said sequence of frame times, selecting M available registers in a packet buffer having B registers, B > M, to store the M input packets simultaneously arriving in the next frame of said sequence

of frame times, setting up connections in an input module to switch the M input packets to the M available registers, transmitting the register addresses of the M available registers to header hoppers, delivering and storing the M input packets to the M available registers simultaneously using the connections of the input module, sending headers from the M input packets to the header hoppers, transmitting the register addresses from the headers of the M input packets to N queues corresponding to destination addresses in the headers of the M input packets simultaneously, updating the queues based on the header information provided by the header hoppers, sending control information to a register selector to inform the register selector of the destination addresses of the M input packets in each frame of said sequence of frame times, selecting up to N stored packets from the packet buffer for each of the destination addresses based on contents of the queues, transmitting the up to N selected stored packets to the outputs simultaneously, updating the register selector to account for any remaining destination addresses for each stored packet, and transmitting any remaining stored packets to the N outputs in subsequent one or more subsequent frames to clear the remaining stored packets" as disclosed in claim 23;

"switching the M input packets to M of the B outputs to produce M switched packets simultaneously during each frame of said sequence of frame times, B > M, storing the M switched packets into M of B registers during each frame of said sequence of frame times to produce M stored packets simultaneously, and transferring up to N packets from up to N of the B registers in each frame of said sequence of frame

times to the output ports simultaneously based upon destination information" as disclosed in claim 24.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Lee whose telephone number is (571) 272-3131. The examiner can normally be reached on Monday through Friday from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing Chan can be reached on (571) 272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew C. Lee/::<5/23/2007>

5/23/07
WING CHAN
SUPERVISORY PATENT EXAMINER